

**NONPROVISIONAL PATENT
APPLICATION TRANSMITTAL RULE §1.53(b)
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Customer No. 004372
ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
1050 Connecticut Avenue, N.W.,
Suite 400
Washington, DC 20036-5339
Telephone: (202) 857-6000
Facsimile: (202) 638-4810

Docket No. 100021-00072
Date: February 26, 2002

Commissioner for Patents
Washington, D.C. 20231

Sir:

Transmitted herewith for filing under 37 C.F.R. §1.53(b) is a nonprovisional patent application:

For (Title): TEST CIRCUIT AND SEMICONDUCTOR INTEGRATED CIRCUIT
EFFECTIVELY CARRYING OUT VERIFICATION OF CONNECTION OF
NODES

By (Inventors): Kohtaroh GOTOH; Koji AOYAGI; Kazuhiro TERASHIMA; Shigeru NISHIO

- ☒ 27 pages of Specification/Claims 1-44/Abstract are attached.
- ☒ Formal drawings (Figs. 1-14; 14 sheets) are attached.
- ☒ A Declaration and Power of Attorney is attached.
- ☒ An assignment of the invention to FUJITSU LIMITED is attached, along with Form PTO-1595 and a check for \$40.00.
- ☒ Priority of foreign application No. 2001-269216 filed September 5, 2001 in Japan is claimed under 35 U.S.C. §119.
- ☒ A certified copy of the above corresponding foreign application is attached.

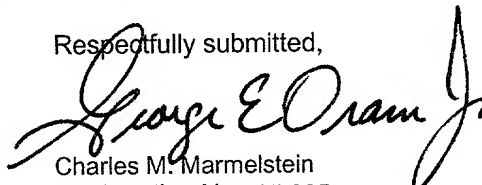
The filing fee is calculated below and includes claim status after entry of any Preliminary Amendment noted above:

FOR:	NO. FILED	NO. EXTRA
BASIC FEE		
TOTAL CLAIMS	44 - 20	= 24
INDEP CLAIMS	4 - 3	= 1
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIMS		

SMALL ENTITY			LARGE ENTITY	
RATE	FEE	OR	RATE	FEE
	\$ 370	OR		\$ 740
x 9 =	\$	OR	x 18	\$ 432
x 42 =	\$	OR	x 84	\$ 84
+140 =	\$	OR	+280	\$
TOTAL	\$	OR	TOTAL	\$ 1256

- ☒ A check in the amount of \$1,296 (\$1,256 for the filing fee and \$40 for the Assignment Recordation Fee) is attached. Please charge any fee deficiency or credit any overpayment to Deposit Account No. 01-2300.

Respectfully submitted,


Charles M. Marmelstein
Registration No. 25,895

CMM/baw

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1002 U.S. PTO
10/082055
02/26/02